Motor Drive Circuits Using the D469A

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Introduction

Many applications operate MOSPOWER devices as on/off switches. In applications where device switching speed is of less concern and the MOSPOWER device's gate capacitance (C_{iss}) is sufficiently low, they may be driven directly by CMOS logic or by a TTL gate with a pull-up resistor. The prime advantage that encourages use of MOSPOWER devices over bipolar transistors, however, is the efficiency gained from reduced on-state voltage drop and increased switching speed. The gate of a MOSPOWER device is capacitive. The value of C_{iss} is directly related to the device size, and switching speed is directly proportional to the gate driver output impedance. To take advantage of the increased switching speed of large MOSPOWER devices, a more robust driver than simple logic devices is required.

The D469A was designed as an optimized driver for MOSPOWER devices. It contains four independent drive channels, and each channel can be configured as a logically inverting or non-inverting driver. Since the D469A is a CMOS device, it is compatible with low-power CMOS logic and microprocessors and draws minimal quiescent current ($\leq$1.0 mA). The D469A switching times (typically 20 ns) are specified with a 500 pF load, but higher capacitive loads may be driven with proportionally increased transition times. Output impedance of the D469A (both pull-up and pull-down) is typically less than 6 Ω, permitting peak charging currents greater than 1.0 A (at low duty-cycles).

Applications of the D469A Quad Driver

The D469A quad driver is well suited to applications such as motor drives. Motors ranging from fractional to integral horsepower can be driven directly with MOSPOWER devices. The D469A provides optimized gate drive signals and simplifies interface to the logic level control circuitry.

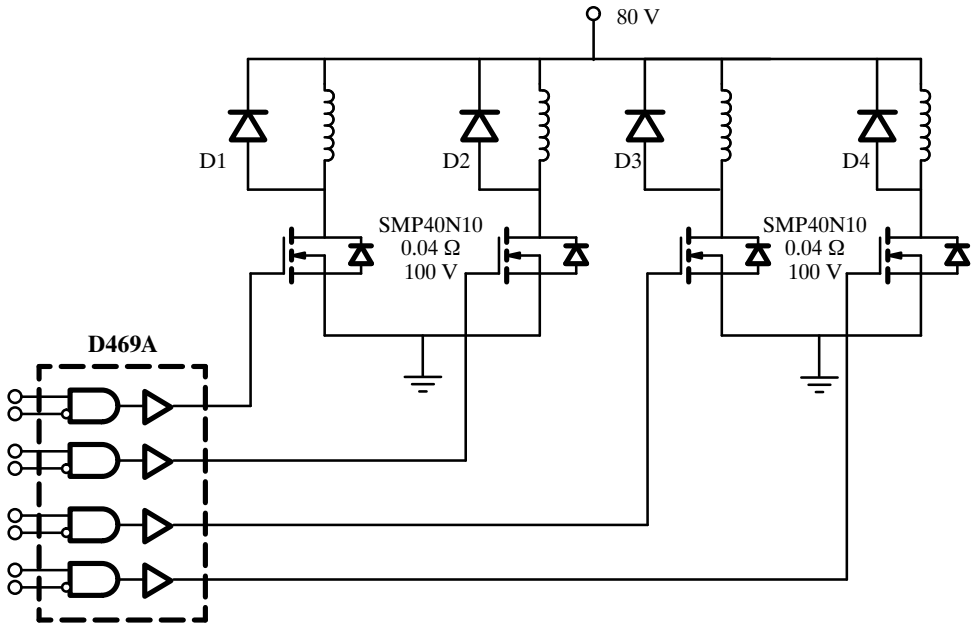

Figure 1. Unipolar MOSPOWER Stepper Motor Drive

Figure 1 illustrates a “unipolar” configuration widely used in stepper motor drives. In this application, the MOSPOWER devices are operated as “low-side” switches with their sources and the D469A gate driver referenced directly to ground. Diodes D1 to D4 protect the MOSPOWER devices from overvoltage as a result of flyback voltage generated by the motor winding when a MOSPOWER device is turned off.

MOSPOWER devices offer distinct advantages in low-voltage motor drive applications. Mobile, battery powered applications such as automotive, aircraft, boats, satellites, missiles, and mobile robotics are improved by the efficiency of MOSPOWER devices. Power consumed during switching transitions decreases motor performance and increases heat that must be dissipated. New low on-resistance MOSPOWER transistors increase current handling capability for a given heat sink or decrease heat sink requirements at any given current level. Using an efficient gate driver like the D469A can further increase efficiency by minimizing quiescent current and transition times as well as providing sufficient gate voltage to minimize the MOSPOWER devices on-state voltage drop.

In Figure 2, a low-voltage H-bridge configuration is demonstrated which provides the motor with bi-directional (bipolar) current drive capability. This arrangement works particularly well in applications that use a single 12-V battery to power the motor and electronics. By using n-channel MOSPOWER devices as “low-side” switches (sources referenced to ground) and p-channel MOSPOWER devices as “high-side” switches (sources referenced to the battery voltage), the gates of all four devices can be driven directly by one D469A quad MOSPOWER driver.

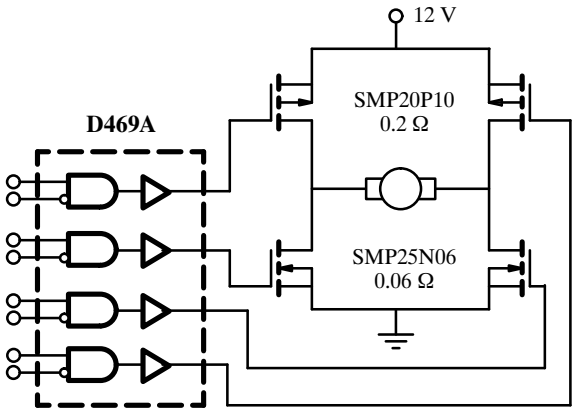

Figure 2. Low-voltage Complementary MOSPOWER H-bridge

As Figure 3 illustrates, driving the gates of p-channel high-side devices in a high-voltage bridge is slightly more complex than the previous low-voltage applications, but still considerably less complex than when n-channel high-side switches are used. Although p-channel devices typically cost more then n-channel devices for a given $r_{DS(on)}$ rating, the added device cost is often offset by the reduced cost of the gate-drive circuitry.

In Figure 3 a depletion-mode MOSFET is used as a linear series regulator to create a power supply which is 12 V below the bridge voltage to supply power for the D469A MOSPOWER gate driver. Current through the series regulator can be calculated based on the average current needed to drive the total gate capacitance at the desired switching frequency plus the quiescent current of the D469A. C_1 is a bypass capacitor which supplies the peak current needed for fast MOSFET switching.

One particular advantage inherent to this drive technique is that it holds the p-channel upper devices “normally off.” Absence of a gate drive signal results in the gate-source of Q_1 clamped in a safe (low-impedance) state. This gate drive technique provides a safe “power-up” condition, as well as additional failure protection should the low-side supply voltage be interrupted during operation.

The “All N-channel” Half-bridge

Bridges using n-channel devices in both the upper and lower switch locations always offer advantages when pushing the “state-of-the-art.” The lowest $r_{DS(ON)}$ and highest breakdown voltage MOSPOWER devices in the marketplace will always be n-channel. N-channel material offers more than twice the current-carrying efficiency (carrier mobility) of p-channel material, per unit area. A p-channel device of comparable current, voltage, and $r_{DS(on)}$ ratings, constructed with comparable cell density, will be more than twice the die area of its n-channel complement.

In Figure 4, a JFET (Q3) is used to provide the p-channel power MOSFET with a low gate-source impedance when turned off. The J107 has an rDS(ON) of less than 10 Ω when the gate-source voltage is greater than zero. Zener diode D1 protects the p-channel power MOSFET gate-source from excessive voltage. Zener diode D3 protects the gate-source of JFET Q3 from excessive voltage when Q4 or Q5 is on. The CR100 (D2) is a constant-current (1.0 mA) diode used to turn the JFET (Q3) on when Q5 is turned off.

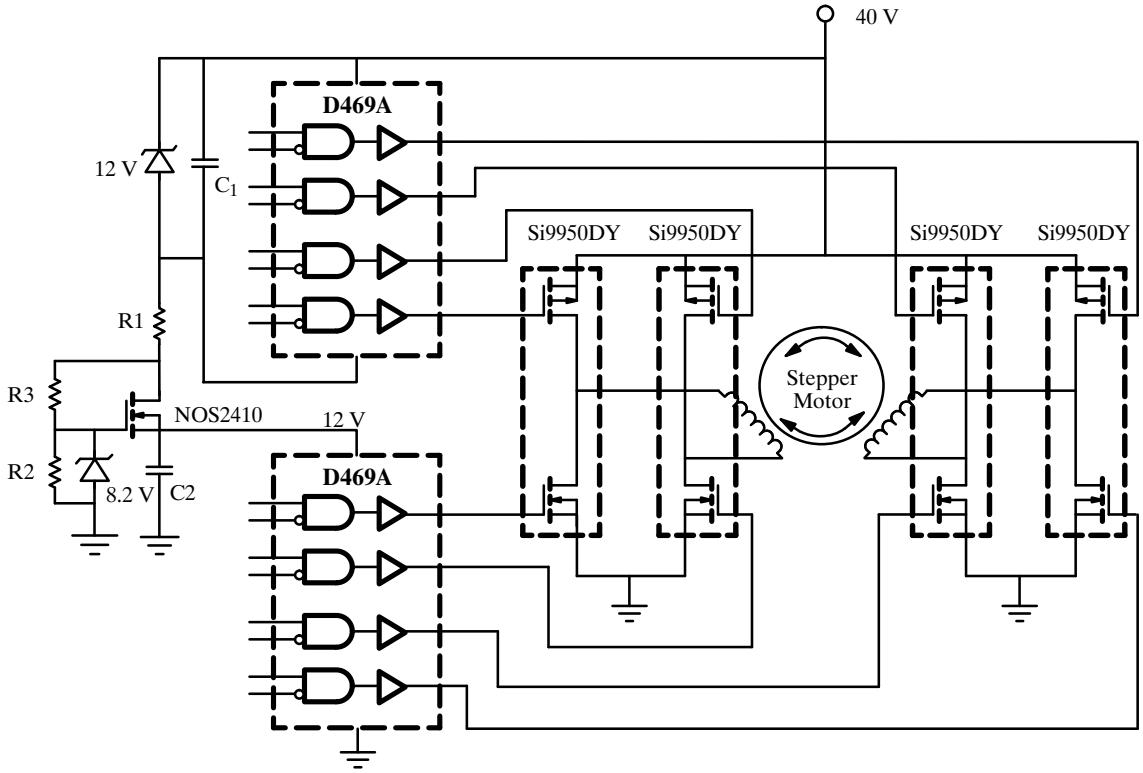

Figure 3. High-Voltage Complementary MOSPOWER H-bridge

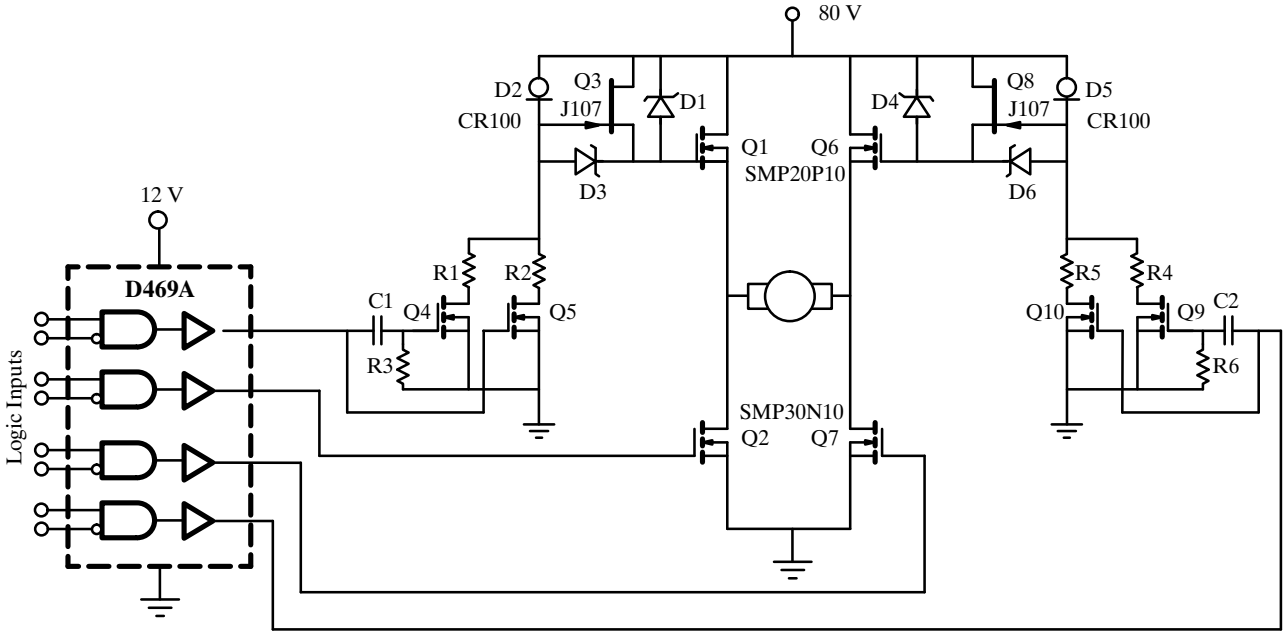

Figure 4. "JFET Clamp" for High-Side P-Channel Gate Drive

Q4, Q5, R1, R2, R3 and C1 form a bi-level current sink used to drive the JFET clamp (Q3) and upper p-channel power MOSFET (Q1). When Q4 and Q5 are driven on by the control logic, they initially source current at a level set by R1 and R2 (R1 is typically much smaller than R2). The peak current through R1 and D3 drives the p-channel gate to a voltage level clamped by diode D1, turning the power MOSFET (Q1) on. After the power MOSFET is turned on, the current-source value is reduced by approximately an order or magnitude to maintain the power MOSFET's enhancement voltage. Peak current timing is set by the time constant of R3 and C1, and the maintenance current level is set by the value of R2.

When the current-sink driver is turned off, constant-current diode D2 pulls the gate of JFET Q3 to the high-voltage rail, turning Q3 on and Q1 off. The p-channel gate is driven off at essentially the same rate as the rise of Q3's gate and held securely off by the low impedance of Q3. JFETs (or n-channel depletion-mode power MOSFETs which could also be used in this circuit) can easily provide on-resistance low enough to prevent transients on the MOSFET's drain (dv/dt) from generating enough voltage at the gate to allow spurious turn-on.

Using n-channel devices in the upper quadrants of the H-bridge complicates gate drive. The gate of the n-channel device must be 10 to 12 V positive (with reference to its source) to turn the device fully on. In a half-bridge, the high-side n-channel device's source may be at any voltage between a diode drop below ground and a diode drop above the motor drive voltage. To drive the gate properly, a separate voltage must be generated that is referenced to the high-side n-channel device's source and capable of going at least 10 V above the motor voltage.

In Figure 5, a high-frequency oscillator (100 kHz) and a small bi-filar-wound pulse transformer are used to form floating 12-V power supplies referenced to the source of each upper n-channel device. The value of supply capacitors C1 and C2 are chosen based on capacitance values of the n-channel gates being driven and the quiescent current of the floating opto-coupler buffer.

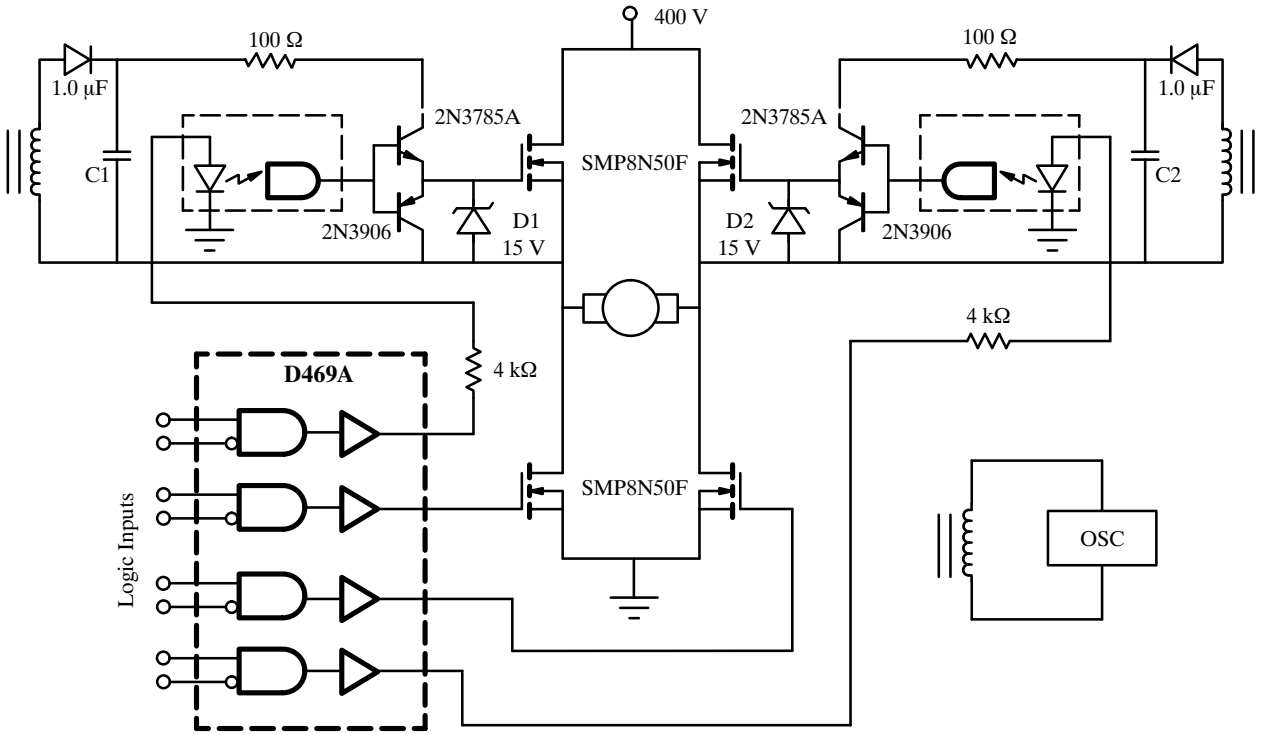

Figure 5. All N-channel Bridge with Opto-coupled Logic Signal

Diodes D1 and D2 are added to protect the power MOSFET gates from overvoltage conditions. An opto-coupler is used to isolate gate-drive signals, and the emitter follower output stage provides the required high peak gate drive currents.

The high-side drive configuration in Figure 5 allows "static" operation. The high-side n-channel devices can be held on in a steady-state condition, providing a switching range from dc to the maximum bridge operating frequency. The oscillator operates continuously to provide power for the two floating gate-drive supplies. In this arrangement, the pulse transformer can be driven at a much higher frequency than the modulation frequency, making the transformer smaller than in configurations that drive the gate directly through a pulse transformer.

A dynamic "bootstrap" gate-drive technique is demonstrated in Figure 6. Dynamic isolation is compatible with several styles of motor drive and current control that result in continuous modulation. If dynamic gate-drive techniques can be applied, they often result in reduced cost by eliminating high-cost items such as high-performance opto-isolators. This configuration has one other inherent feature when compared to the floating power supply technique discussed previously. When an upper MOSPOWER device is turned off, its gate is clamped to its source (by low-impedance p-channel device Q2) to prevent spurious dv/dt turn-on (see *Siliconix MOSPOWER Applications Handbook*, "dvDS/dt Turn-on in MOSFETs").

In operation, when Q1 is turned on, the p-channel clamp (Q2) assures that the gate-source of Q4 remains shorted. While Q1 is on, Q5 (the lower output MOSPOWER device) will be turned on. The bootstrap capacitor is then charged from the low-voltage supply via D1 and Q5. When Q1 is turned off, Q2 is also turned off, releasing the clamp across Q4's gate-source. R1 is allowed to pull the gate of Q3 high, turning it on. This switches current into the capacitive gate of Q4 via Q3 and D3. As Q4 begins to turn on, voltage at the source begins to rise toward the positive motor drive voltage.

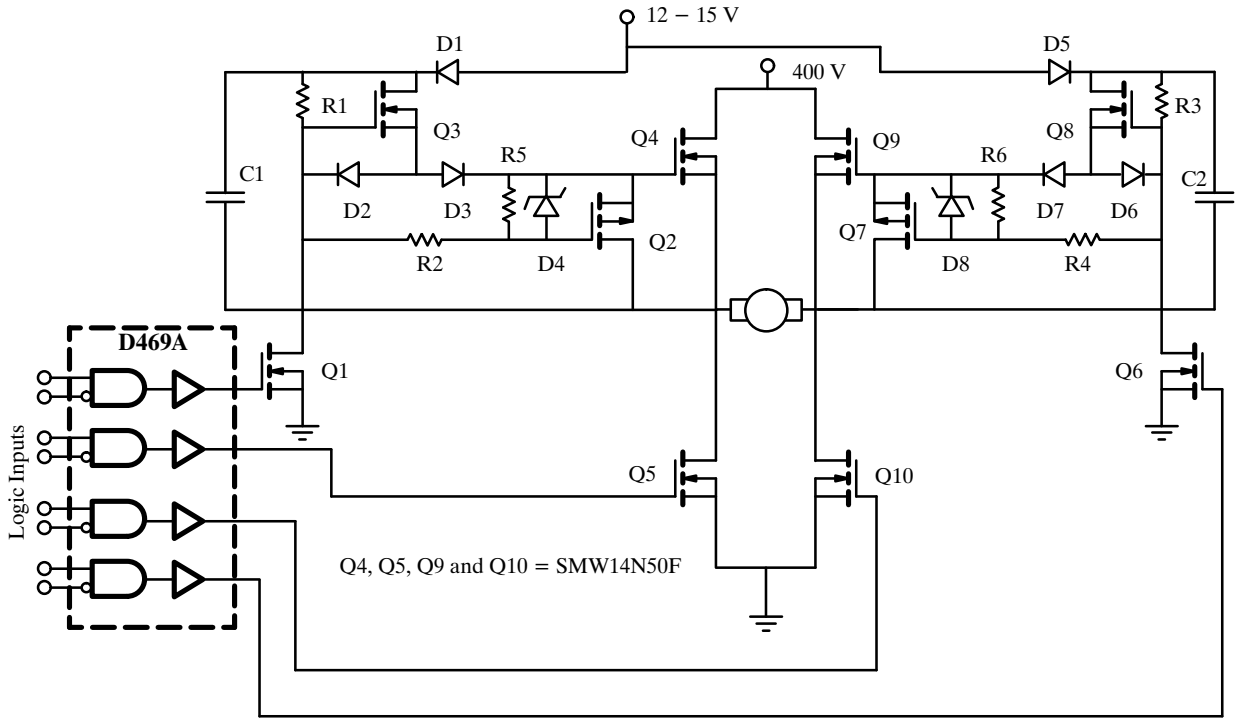

Figure 6. Bootstrap High-side N-channel Gate Drive Isolation

As it rises, it carries with it the reference (low) end of the bootstrap capacitor. D1 (which must be a fast-recovery diode) reverses, protecting the bootstrap capacitor's charge. Above this point, remaining gate charge must be supplied by the bootstrap capacitor, which must be at least an order of magnitude larger than the MOSPOWER gate capacitance (Q4) being driven. When the upper MOSPOWER device (Q4) is fully enhanced, the source will be below the motor drive voltage by an amount equal to $V_{DS} = I_D \times r_{DS(ON)}$, and its gate will be held at the voltage potential remaining in the bootstrap capacitor minus the voltage drop through Q3 and D3. The leakage currents of D1, Q1, Q2 and Q4 will limit the amount of time a high level can be maintained without allowing the stored capacitor voltage to "droop" to a dangerous voltage level. As a general rule, 8 V is a reasonable (absolute minimum) gate-drive voltage to allow. With less than 8 V of gate drive, the rDS(ON) of Q4 will increase rapidly, increasing power dissipation and motor drive voltage losses.

Summary

Designing a power MOSFET bridge for a motor drive, as with any power circuit, involves an understanding of economic and performance requirements. Both will impact the selection of an "optimized" gate drive technique for the MOSPOWER devices. Some methods of isolating the high-side gate drive are advantageous at low voltages but become inefficient or otherwise unsatisfactory at higher voltages. Other isolation techniques work well over a wide range of voltages but are less economical. Still others provide economic advantages but are incompatible with the controller's modulation scheme. Each isolated high-side gate drive technique will be well suited to a range of applications and less than optimum in others. As demonstrated in this applications note, most of these gate drive circuits can benefit from a flexible and economical integrated circuit such as the D469A CMOS quad driver.